3-7 — Relationship of Voltage Breakdown and Switching Load Lines

The conventional methods of specifying transistor voltage breakdown do not provide the designer very much data to actually determine that a switching load line will remain free of the avalanche voltage breakdown region. Although the BV_{CNO} specification does provide a maximum collector voltage limit, there is no assurance that the voltage-current excursions of a switch being turned off to BV_{CBO} will not enter the avalanche region. Figure 3-15 is a comprehensive transistor characteristic graph showing the avalanche region characteristics in addition to the normal operating characteristics. The breakdown characteristics switch back from BV_{CBO} towards BV_{CEO}.

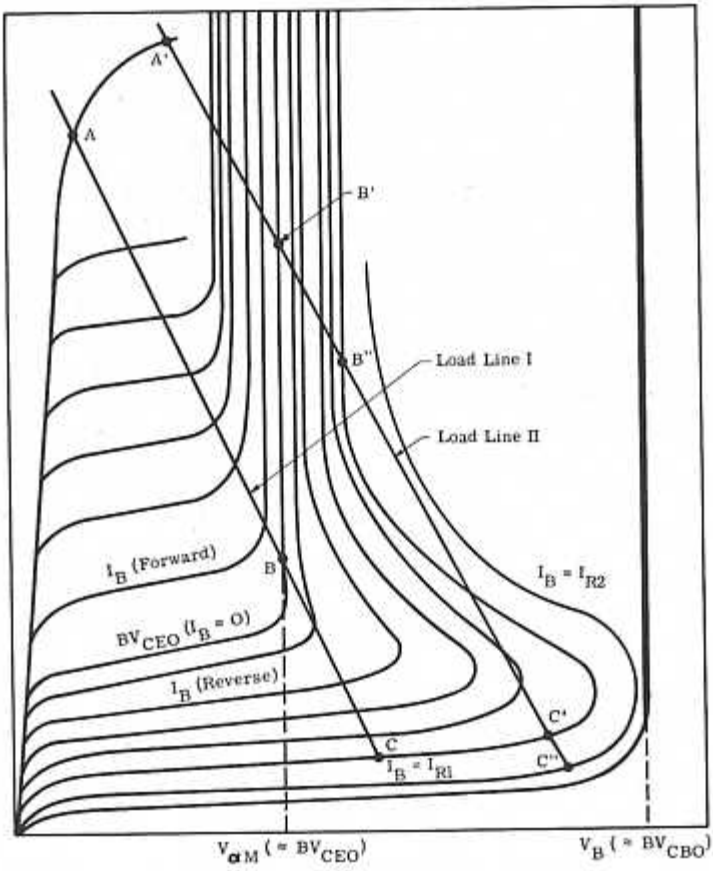

Figure 3-15 — Comprehensive Transistor Characteristics

If the load line of a switching circuit intercepts any of these curves in the breakdown region, it is possible that a stable operating point will result in the breakdown region. Examine the turnoff of a transistor switch with load line I and an on point at A. As drive is reduced, the operating point moves down the

load line, each intersecting point corresponding to an intersection of the load line with a collector current line determined by the base current at that instant. When $I_B = 0$, operation is at Point B, in the avalanche region. However, as reverse base current is increased to the final value I_{B1}, operation moves to Point C in the cutoff region. Examine load line 11 with an on condition point of A′. As current is reduced to zero, operation moves to B′ in the avalanche region. However, in this case the application of reverse bias which has the same final value of I_{B1} only moves operation to B″ in the avalanche region instead of to the desired off point, C′. The transistor is then in a condition which is called latch-up as it is locked at a stable on point in the avalanche region. The collector voltage has not reached the desired off value and the collector current is much greater than I_{CL}. Latch-up not only causes circuit malfunction, but could result in damage to the transistor, if the product of voltage and current at the point of latch-up is high enough to exceed the power ratings of the transistor. To allow the transistor to turn off, the reverse base current is increased to I_{B2}. There is now only one intersection of the load line with the base current curve and it is at point C″.

Since breakdown voltage specifications alone are not sufficient to forecast "latch-up" conditions, charts similar to the one shown in Figure 3-16 have been devised to provide a method of checking switching circuit load lines. This chart has three discrete areas indicated (1) a safe or latch-free load line area, (2) a conditionally safe area of operation, and (3) a forbidden or latch-up area.

The part of several representative load lines during turn off are shown on Figure 3-16 which applies to a 2N964A transistor. Load line "A" is a resistive load line and it lies entirely within the latch-free load line area. Load line "B" is also a resistive load, but it transverses the conditionally safe area, and could cause trouble if the fall time of the output pulse exceeds 15 nanoseconds. Load line "C" is a capacitive load line (collector current leads the collector voltage).

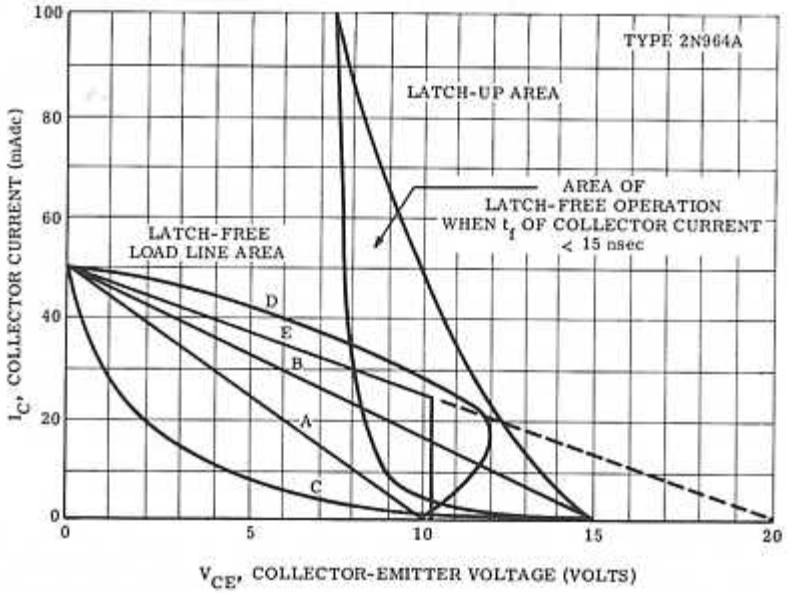

Figure 3-16 — Area of Permissible Load Loci Chart with Representative Load Lines

Capacitive load lines, generally, are latch-free since they have a shape such that they slip under the conditional area. Increasing turn off current (I_{B2}) increases the capacitive effect.

Load line "D" is an inductive load line because voltage leads the current. It also exhibits an inductive "kick". To be trouble-free, the fall time must be less than 15 nanoseconds. However, if the fall time is slower than 15 nanoseconds, latch-up conditions would depend upon the resistive component of the load line. For example, if the resistive component is load line "A", there will be a temporary latch-up condition until the energy in the inductance is dissipated. This temporary latch-up would result in an abnormally long fall time and considerable peak power dissipation. However, the transistor would eventually turn off.

The remaining load line "E" is the load line of an output circuit which uses a clamp diode to establish the off level. Since this load line lies within the conditionally safe area, the fall time must be less than 15 nanoseconds.

If an Area of Permissible Load Loci Chart is not supplied, one can be constructed by conducting tests on some low voltage transistor samples. Generally, it is necessary for the circuit designer to check individual circuits, using low limit BV_{CEO} samples to determine if latch-up can occur. To provide a more complete picture of the relationship of transistor voltage breakdown ratings and latch-up, the following section is a brief review of voltage breakdown in transistors.

3-8 — Avalanche Breakdown Theory

Avalanche breakdown occurs when the reverse bias applied to a semiconductor junction produces an electric field in excess of approximately 10^5 volts per centimeter. Under this condition, carriers are accelerated sufficiently to excite additional carriers by impact ionization with the atoms in the crystal lattice. Since this occurs at high fields and therefore high carrier velocities, recombination can be neglected, and the effect is regenerative.

This process can be described by the multiplication factor previously discussed (M) which Miller[2] has shown to be approximately

$$M = \frac{1}{1 - \left(\frac{V}{V_B}\right)^m} \qquad (3\text{-}14)$$

Where: $V =$ the applied voltage

$V_B =$ the avalanche breakdown voltage (See Note 1)

$m =$ empirical determined constant

A graph of this relationship is shown in Figure 3-9, where M is plotted as a function of the voltage ratio V/V_B. As $V \rightarrow V_B$, M increases without limit.

Note 1

The actual collector-base breakdown voltage is defined as V_B and the collector-emitter breakdown as V_{BM}. These terms refer to the true breakdown voltages, i.e., to a voltage which will cause an infinite, or nearly so, increase in current if exceeded. It is common to measure V_B in a circuit with the emitter open and with a constant current forced through the junction. This is called a BV_{CBO} test. Note, however, from Figure 3-15, that the current used for the test must be large enough to put the operating point over the knee, or the true breakdown voltage, V_B will not be measured. The same general comment is true regarding BV_{CEO} and V_{BM}. Both BV_{CBO} and BV_{CEO} represent a locus of points, while V_B and V_{BM} represent a definite breakdown voltage.

Tests designated BV_{CEX} and BV_{CER} are also used. The symbol x indicates some reverse bias and resistance are used from base to emitter (which must be specified) while R indicates a resistance alone is used.